## REMARKS

Claims 1-42 are pending. Claims 1, 12, 23, 34 and 42 have been amended.

In paragraph 3 on page 2 of the Office Action, claims 1, 12, 23, 34 and 42 were rejected under 35 U.S.C. § 103 (a) as being unpatentable over Belsan et al. in view of Johnson.

In paragraph 7 on page 3 of the Office Action, claims 2-8, 10-11, 13-19, 21-22, 24-30, 32-33 and 35-41 were rejected under 35 U.S.C. § 103 (a) as being unpatentable over Belsan et al. in view of Johnson and further in view of Moriyama et al.

In paragraph 17 on page 5 of the Office Action, claims 9, 20 AND 31 were rejected under 35 U.S.C. § 103 (a) as being unpatentable over Belsan et al. in view of Johnson and further in view of Stuttard et al.

Applicants traverse the above rejections, but in the interest of expediting prosecution have amended the claims to more particularly define the invention over the cited references.

Belsan et al. fail to disclose a plurality of controllers wherein each controller includes a CPU for controlling the operation of a controller, program memory, coupled to the CPU, for storing program instructions and variables for the operation of the CPU and cache memory, coupled to the CPU, for storing information related to the array of storage devices. The Office Action indicates the the pluralty of controllers are disclosed in Belsan et al. by host 11 and 12 and data storage subsystem 100. However, hosts 11 and 12 do not show a CPU for controlling the operation of a controller, program memory, coupled to the CPU, for storing program instructions and variables for the operation of the CPU and cache memory, coupled to the CPU, for storing information related to the array of storage devices.

Moreover, Belsan et al. fail to disclose, teach or suggest a task coordination data object that consists of discrete partitions of a task comprising task instructions and states for each partition of the task.

Rather, Belsan et al. merely disclose a method for modifying a virtual track in cache rather than at the physical location of the data on a storage device. According to Belsan et al., to perform a write operation, the virtual track that contains the data record to be rewritten is staged from the logical layer into the cache memory 113. Modified data record is then transferred into the virtual track and this updated virtual track instance is then scheduled to be written from the cache memory 113 where the data record modification has taken place into the logical layer. All of the data updating is performed in the cache memory 113, and the virtual track in which this data is to be written must be transferred from the redundancy group in which it is stored to the cache memory 113 if it is not already resident in the cache memory 113.

The copy of the virtual track that resides in the redundancy group is then rendered inaccurate and must be removed from access by the host processors 11-12. Once this merge of the modified record data into the original virtual track instance has been completed and the virtual track now is updated with the modified record data received from host processor 11, the updated virtual track instance must be scheduled for writing onto a redundancy group. Whether the virtual track instance as updated fits into an available open logical cylinder is determined. Finally, the virtual track instance as updated is written to free logical cylinder.

As can be seen then, Belsan et al. does not disclose anything concerning a task coordination data object that consists of discrete partitions of a task comprising task instructions and states for each partition of the task.

Still further, from the above description of Belsan et al. it is clear that Belsan et al. fails to disclose that task instructions for each partition of the task are capable of being completed separately by one of the plurality of controllers to allow the task to be completed by way of the cummulative effort of the plurality of controllers completing seaprately the partitions of the task.

Belsan et al. simply fails to suggest cummulative effort of the plurality of controllers is used for completing seaprately the partitions of the task.

Yet even further, Belsan et al. fails to disclose that a free controller of the plurality of controllers selects a partition of the task available for completing separately and independently of the other controllers as indicated by the states for each partition of task instructions. Belsan et al. simply fail to recognize the advantages of using separate controllers to complete sub-portions of a task.

Accordingly, Belsan et al. fail to disclose, teach or suggest the elments recited in the indepentent claims as amended.

Johnson faiils to overcome the deficiencies of Belsan et al. Johnson is merely cited as disclosing the use or processor modules to perform independent tasks to a memory subsystem. However, Johnson does not suggest dividing a task into discrete partitions of task instructions, wherein the task instructions for each partition of the task are capable of being completed separately by one of the plurality of controllers to allow the task to be completed by way of the cummulative effort of the plurality of controllers completing seaprately the partitions of the task.

In addition, Johnson does not teach the plurality of controllers as claimed.

Accordingly, Belsan et al. and Johnson, alone or in combination, fail to disclose, teach or suggest the elments recited in the indepentent claims as amended.

Moriyama et al. fails to overcome the deficiencies of Belsan et al. and Johnson. Moriyama et al. are merely cited as disclosing states for tasks. However, as with Belsan et al. and Johnson, Moriyama et al. fails to suggest dividing a task into discrete partitions of task instructions, wherein the task instructions for each partition of the task are capable of being completed separately by one of the plurality of controllers to allow the task to be completed by

way of the cummulative effort of the plurality of controllers completing seaprately the partitions of the task.

In addition, Moriyama et al. do not teach the plurality of controllers as claimed.

Accordingly, Belsan et al., Johnson and Moriyama et al., alone or in combination, fail to disclose, teach or suggest the elments recited in the indepentent claims as amended.

Stuttard fails to overcome the deficiencies of Belsan et al., Johnson and Moriyama et al. Stuttard is merely cited for the teaching of a semphore mechanism. However, Stuttard also fails to suggest dividing a task into discrete partitions of task instructions, wherein the task instructions for each partition of the task are capable of being completed separately by one of the plurality of controllers to allow the task to be completed by way of the cummulative effort of the plurality of controllers completing seaprately the partitions of the task.

In addition, Stuttard does not teach the plurality of controllers as claimed.

Accordingly, Belsan et al., Johnson, Moriyama et al., and Stuttard, alone or in combination, fail to disclose, teach or suggest the elments recited in the indepentent claims as amended.

Therefore, Applicants respectfully submit that claims 1, 12, 23, 34 and 42 are patentable over the cited references.

Dependent claims 2-11, 13-22, 24-33 and 35-41 are also patentable over the references, because they incorporate all of the limitations of the corresponding independent claims 1, 12, 23 and 34 respectively. Further dependent claims 2-11, 13-22, 24-33 and 35-41 recite additional novel elements and limitations. Applicants reserve the right to argue independently the patentability of these additional novel aspects. Therefore, Applicants respectfully submit that dependent claims 2-11, 13-22, 24-33 and 35-41 are patentable over the cited references.

On the basis of the above amendments and remarks, it is respectfully submitted that the claims are in immediate condition for allowance. Accordingly, reconsideration of this application and its allowance are requested.

If a telephone conference would be helpful in resolving any issues concerning this communication, please contact Attorney for Applicant, David W. Lynch, at 423-757-0264.

Respectfully submitted,

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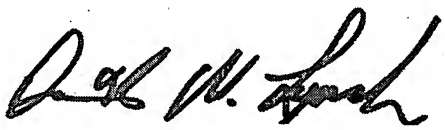
By: 

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